IN THE CLAIMS

A marked up version of the claims as amended is set forth below.

Please amend the claims as follows:

1. (Currently amended) A computer peripheral device comprising:

a memory for storing a configuration address; and

a power level control circuit for controlling the power level in the device so as to be in a standby mode or normal power mode after power is applied to the device, the circuit being ~~couple~~ coupled to the memory to cause the memory to store the configuration address from a bus when the device enters [[a]] the normal power mode.

2. (Currently amended) The device defined by claim 1 wherein the memory, once storing a configuration address, retains that address until the device is reset or the power is turned on or off.

3. (Currently amended) The device defined by claim [[2]] 1 wherein the memory does not change its stored address when the device is reconfigured.

4. (Original) The device defined by claim 3 wherein the bus is an address bus.

5. (Currently amended) The device defined by claim 4 wherein the memory restores an address after a reset signal is received by the circuit or the power is turned on or off.

6. (Original) The device defined by claim 5 wherein the circuit is responsive to two addresses once a configuration address is stored.

7. (Currently amended) The device defined by claim 1 wherein the memory restores an address after a reset signal is received by the circuit or the power is turned on or off.

8. (Currently amended) A computer system comprising:

a processor; and

a plurality of peripheral devices coupled to the processor through at least one bus, each device having a power level control circuit for causing the device to be in a standby mode or normal operating mode once power is applied to the device and a storage circuit for storing a configuration address, the storage circuit storing a configuration address from the bus when the power level control circuit initially ~~powers up~~ causes the device to be in [[a]] the normal operating mode.

9. (Original) The system defined by claim 8 wherein the bus is an address bus.

10. (Currently amended) The system defined by claim 8 wherein each of the peripheral devices [[are]] is initially sequentially brought into a normal operating mode from a standby mode.

11. (Currently amended) The system defined by claim 10 wherein the peripheral devices are sequentially ~~powered up~~ brought into the normal operating mode after a reset or after power is turned on or off.

12. (Currently amended) A computer system comprising:

a processor;

an output unit coupled to the processor; and

a plurality of peripheral devices each being coupled to a bus and each being coupled to a power level control line from the output unit, signals over each control line causing each device to be placed in a standby mode or normal operating mode after power is applied to the device, each peripheral device having a memory which receives and stores a configuration address from the bus in response to [[a]] the signal on its respective power level control line ~~causing~~ which causes the device to enter [[a]] its normal operating mode.

13. (Original) The system defined by claim 12 wherein the bus is coupled between the output unit and the peripheral devices.

14. (Original) The system defined by claim 13 wherein the bus is an address bus.

15. (Currently amended) The system defined by claim 12 wherein the memory of each of the peripheral devices store a configuration address only when first entering the normal operating mode after a reset or after the power is turned on or off.

16. (Currently amended) A method for operating a computer system comprising:

applying power to a plurality of peripheral devices;

entering a power standby mode in the plurality of peripheral devices;

sequentially entering a normal power mode from [[a]] the standby mode for each of the peripheral devices; and

storing a unique configuration address [[is]] in each device as each enters the normal power mode.

17. (Original) The method defined by claim 16 wherein the storing step occurs after reset.

18. (Currently amended) The method defined by claim [[17]] 16 wherein the storing step for each peripheral device includes the reading of data from a bus.

19. (Currently amended) The method defined by claim 18 wherein the reading of data from a bus comprises the reading of data from [[an]] a data bus and an address from an address bus.

20. (Original) The method defined by claim 18 including configuring each peripheral device after it has stored its configuration address.